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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of	)	
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JIANG et al.	)	
	)	
Application Number: 10/767,444	)	**Art Unit 2186**
	)	
Filed: January 30, 2004	)	
	)	
For: DISK ARRAY DEVICE AND CONTROL METHOD OF DISK ARRAY DEVICE	)	
	)	
Attorney Docket No. ASAM.0099	)	

Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

PETITION TO MAKE SPECIAL UNDER 37 C.F.R. § 1.102(d)

FOR ACCELERATED EXAMINATION

Sir:

Pursuant to 37 C.F.R. § 1.102(d), Applicant respectively requests the application to be examined on the merits in conjunction with the pre-examination search results, the detailed discussion of the relevance of the results and amendments as filed concurrently.

Substantive consideration of the claims is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

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March 17, 2005
SPF/JCM/JT

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STATEMENTS & PRE-EXAMINATION SEARCH REPORT SUPPLEMENTAL TO THE PETITION TO MAKE SPECIAL

Sir:

Pursuant to 37 C.F.R. §§ 1.102 and MPEP 708.02 VIII, Applicants hereby submit that (1) all claims of record are directed to a single invention, or if the Office determines that all the claims presented are not obviously directed to a single invention, will make an election without traverse as a prerequisite to the grant of special status; (2) a pre-examination search has been conducted according to the following field of search; (3) copies of each reference deemed most closely related to the subject matter encompassed by the claims are enclosed; and (4) a detailed discussion of the references pointing out how the claimed subject matter is patentable over the references is also enclosed herewith.

FIELD OF THE SEARCH

The field of search covered Class 711, subclasses 111 (U.S. & Foreign), 113 (U.S. & Foreign) and 118 (U.S. & Foreign). Additionally, a computer database search was conducted on the USPTO systems EAST and WEST and a keyword search was also conducted in Class 710,

subclasses 33 (U.S. & Foreign), 107 (U.S. & Foreign) and 112 (U.S. & Foreign). Examiner David Robertson in Class 711 (Art Unit 2186) was consulted in confirming the field of search.

The search was directed towards a disk array device and control method of disk array device. In particular, the search was directed towards claims 1-16 of patent application 10/767,444. The claims describe a plurality of hard disk drives and channel control units for performing data transfer and reception between these units, a plurality of disk control units for performing data transfer and reception between these units, a cache memory for storage of data being transferred and received between channel control units, providing access to the cache memory by use of a certain number of or ones of the data buses which is determined in accordance with a transfer data length that is set in the access request and as further claimed in claims 1-16 in the disclosure provided.

LIST OF RELEVANT REFERENCES

The search revealed the following U.S. and foreign patents, which are listed for convenience:

U.S. Patent Number	Inventor(s)
5,014,194	Itoh
5,640,600	Satoh et al.
6,182,112	Malek et al.
6,493,774	Suzuki et al.
6,587,905	Correale et al.

Published Patent Application	Inventor(s)
2004/0010659	Inoue
2004/0250003	Chang

Foreign Patent Numbers	Inventor(s)
JP 08-137630	Ichikawa et al.

Discussion of References:

U.S. Patent Number 5,640,600 to **Satoh** et al. shows a storage controller 2 and bus control method for use therewith. The buses are used to transfer the data and the control

information between the cache memory 24 and the control memory 25, and the channel adapter 521a and the storage device adapter 522 (Abstract; Fig. 1). **Satoh** involves only one CPU 1 (Fig. 1) such that there were no SAN, or "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. **Satoh's** channels are not serial computer buses, e.g., fiber channels, intended for connecting high speed storage devices to computers via storage area networks in enterprise storage. Beside the essential structural differences, the controller 2 comprises bus load estimating means 201 and bus mode selecting means 203. The storage device adapters control data transfer between the storage devices 3 and the cache memory 24, the bus mode selecting logic part 203 carries out a bus mode selecting process, i.e., the part determines the mode in which to utilize each of the buses and on the basis of the bus activity ratios (col. 7, lines 40+), rather than based upon "a transfer data length being set in the access request" or "an access type indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30". **Satoh's** controller 2 does not respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request" as now recited in claims 1 & 8, or provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15

U.S. Patent Application Number 2004/0010659 of **Inoue** describes an external storage subsystem with channel units and or the control units 70 and 71 that select the cache unit 80 or 81 or the nonvolatile memory unit 90 or 91 by driving a SEL (0-1) signal line ([0047]). **Inoue** involves only one CPU 1 (Fig. 1) such that there were no SAN, or "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. **Inoue's** channels are not serial computer buses, e.g., fiber channels, intended for connecting high speed storage devices to computers via storage area networks in enterprise

storage. Beside the essential structural differences, the controller 70 or 71 or the channel unit 60 or 61 merely specifies a status of the data buses from 60A through 71B, by a combination of the signals in a general manner ([0047]), rather than based upon "a transfer data length being set in the access request" or "an access type indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30". **Inoue's** controller 70 or 71 does not respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request" as now recited in claims 1 & 8, or provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15.

U.S. Patent Number 5,014,194 to **Itoh**'s data processing system (Fig. 1) only one CPU 25 (Abstract; Fig. 1) such that there were not any SAN, or "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. **Itoh's** channels are not serial computer buses, e.g., fiber channels, intended for connecting high speed storage devices to computers via storage area networks in enterprise storage. Beside the essential structural differences, **Itoh's** data bus controller 68 does not control bus traffic to any cache, nor respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request" as now recited in claims 1 & 8, or provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15.

U.S. Patent Number 6,182,112 to **Malek** et al. only describes a control mechanism within a general purpose digital computer (col. 1, lines 20-23), rather than between any disk array and a plurality of information processing apparatuses connected via a SAN such that there were no "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. **Malek's** channels are not serial computer buses, e.g., fiber channels, intended for connecting high speed storage devices to computers via storage area networks in enterprise storage. Beside the essential structural differences, **Malek's** state machines 44 and 46 only balance between the in-bound and out-bound traffic of the address interface 40 and a data interface 42 (col. 7, lines 63-66; Fig. 2), but do not control bus traffic to any cache, nor respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request" as now recited in claims 1 & 8, or provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15.

U.S. Patent Number 6,493,774 to **Suzuki** et al. only describes a control mechanism within a microcomputer (Fig. 1), rather than between any disk array and a plurality of information processing apparatuses connected via SAN such that there were no "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. **Suzuki's** channels are not serial computer buses, e.g., fiber channels, intended for connecting high speed storage devices to computers via storage area networks in enterprise storage. Beside the essential structural differences, **Suzuki's** bus state control 5 (col. 6, lines 26-33) and the cache TLB controller 44 (col. 5, lines 57-59; col. 7, lines 40-43) do not control bus traffic to any cache, nor respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance

with a transfer data length being set in the access request" as now recited in claims 1 & 8, or provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15.

U.S. Patent Number 6,587,905 to **Correale** et al. only describes a bus controlling mechanism within a computer (Fig. 6), rather than between any disk array and a plurality of information processing apparatuses connected via SAN such that there were no "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. Beside the essential structural differences, **Correale** uses signals to control bus traffic (col. 4, lines 53-67). However, **Correale** do not respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request" as now recited in claims 1 & 8, or provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15.

U.S. Patent Application Number 2004/0250003 of **Chang** only describes a bus controlling mechanism within a computer (Fig. 1; abstract), rather than between any disk array and a plurality of information processing apparatuses connected via SAN such that there were no "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. Beside the essential structural differences, **Chang's** bus arbiter 16 ([0015]) simply do not respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request" as now recited in claims 1 & 8, or

provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15.

Japanese Publication Number JP 08-137630 of **Ichikawa** et al. involves only one computer 17 (Fig. 1) such that there are no SAN, or "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" as now recited in claims 1, 8 & 15. Beside the essential structural differences, **Ichikawa's** memory 5 for storing tentatively data is connected to a data transfer control means (DMAC) 6 for controlling the data transfer among the host interface (Abstract) via a plurality of buses/passes 204 (Fig. 3; [0024]). The buses/passes 204 merely transfer data in parallel ([0030]) without any transmission coordination based upon "a transfer data length being set in the access request" or "an access type indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30". **Ichikawa's** data transfer control means (DMAC) 6 does not respond "to an access request to said cache memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request" as now recited in claims 1 & 8, or provide "access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30) being set in the access request" as now recited in claim 15

CONCLUSION

Based on the results of the comprehensive prior art search as discussed above, Applicants contend that the position calculation method as now recited in independent claim 1, especially the features of "channel control units for data transmission between these units and a plurality of information processing apparatuses communicably connected thereto through a *storage area network*" and "a data transfer integrated circuit responding to an access request to said cache

memory from one of said channel control units, said disk control units and said CPU, for providing access to said cache memory using more than one of said data buses, a number of which is determined in accordance with a transfer data length being set in the access request," and "a data transfer integrated circuit providing access to said cache memory of said second controller by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type (i.e., indicative of whether the access request is from any one of said channel control units and said disk control units or from said CPU)" are patentably distinct from the cited prior art references.

In particular, as now recited in the claim 1 (e.g., as shown in the embodiment of Fig. 1), the disk array device 15 of the invention, comprises: a plurality of hard disk drives 90; a plurality of channel control units 40 for performing data transfer and reception between these units 40 and a plurality of information processing apparatuses 10 being communicably connected thereto through a storage area network; a plurality of disk control units 50 for performing data transfer and reception between these units 50 and said plurality of hard disk drives 90 as communicably connected thereto; a CPU 30 for performing control of said plurality of channel control units 40 and said plurality of disk control units 50; a cache memory 70 for storage of data being transferred and received between said channel control units 40 and said disk control units 50; and a data transfer integrated circuit 60 communicably connected via more than one bus 80 to said channel control units 40, said disk control units 50 and said CPU 30 and also connected via a plurality of data buses 61, 62 to said cache memory 70. The data transfer integrated circuit 60 is responsive to an access request to said cache memory 70 from one of said channel control units 40, said disk control units 50 and said CPU 30, for providing access to said cache memory 70 using more than one of said data buses 61, 62, a number of which is determined in accordance with a transfer data length being set in the access request.

The invention, as now recited in claim 8, is also directed to a control method for the disk array device 15 recited in claim 1. An operation in said data transfer integrated circuit 60 includes the steps of: receiving an access request to said cache memory 70 from any one of said

channel control units 40, said disk control units 50 and said CPU 30; selecting certain one or ones of said data buses 61, 62, a number of which is determined in accordance with a transfer data length being set in the access request; and using the selected data bus to thereby provide access to said cache memory 70.

The invention (e.g. Fig. 10), as now recited in claim 8, is also directed to a disk array device comprising: a first controller 1001 and a second controller 1002 each including the elements of the disk array device recited in claim 1. The data transfer integrated circuit 60 of said first controller 1001 and the data transfer integrated circuit 60 of said second controller 1002 are communicably connected together. The data transfer integrated circuit 60 of said first controller 1001 transfers, when an access request to said cache memory 60 of said second controller 1002 from any one of said channel control units 40, said disk control units 50 and said CPU 30, an access request toward said data transfer integrated circuit 60 of said second controller 1002, which request sets therein an access type indicative of whether the access request is from any one of said channel control units 40 and said disk control units 50 or from said CPU 30. The data transfer integrated circuit 60 of said second controller 1002 is responsive to said access request from said data transfer integrated circuit 60 of said first controller 1001, for providing access to said cache memory 60 of said second controller 1002 by use of a specified number of ones of said data buses, which number is determinable in accordance with said access type being set in the access request.

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable consideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance

of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and phone number indicated below.

Respectfully submitted,

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